molecular beam epitaxy (MBE), chemical vapor deposition (CVD) or other epitaxial techniques. The high k dielectric layer is thick enough to have a leakage current blocking capability equivalent to a ten angstrom thick layer of SiO_2. The appropriate thickness of the high k dielectric layer can be determined as follows. The thickness of the high k dielectric layer is defined by the boundary equation $e_1E_1 = e_2E_2$, where e is a dielectric constant and E is the electric field, given by the applied bias in volts divided by the material thickness. The boundary equation therefore simplifies to $e_1/t_1 = e_2/t_2$, where t is the material thickness. For a given high k material, the required thickness can be determined by plugging in the dielectric constant of SiO_2 and a ten angstrom thickness of SiO_2 on the left hand side of the equation, plugging in the dielectric constant of the selected high k material, then solving for t_2.

IN THE CLAIMS

Also, please amend the remaining claims as shown. Appendix B is attached hereto showing the changes to the claims; language that has been added is shown with underlining and language that has been deleted is shown in brackets.

2. (Amended) The device of Claim 20 wherein each of the dielectric layer, the diffusion barrier layer, and the blocking layer comprise epitaxial layers.

3. The device of Claim 20 wherein the gate electrode comprises silicon germanium.

4. (Amended) The device of Claim 20 wherein each of the diffusion barrier layer and the blocking layer comprise silicon.

5. The device of Claim 20 wherein each of the source/drain regions comprises silicon germanium.

6. The device of Claim 5 wherein each of the source/drain regions comprises amorphous silicon germanium.

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7. The device of Claim 20 wherein the dielectric layer is selected from the group consisting of oxides of zircon, oxides of titanium, oxides of tantalum, and oxides of hafnium.

B4

8. (Amended) The device of Claim 20 wherein the blocking layer comprises less than or equal to ten atomic monolayers.

D1

9. (Amended) The device of Claim 20 wherein the diffusion barrier layer comprises less than or equal to ten atomic monolayers.

11. The device of Claim 21 wherein the gate electrode comprises a metal.

12. The device of Claim 21 wherein each of the source/drain regions has a depth into the well of about 100 to about 1000 Angstroms.

13. The device of Claim 21 wherein the source/drain regions comprise amorphous material.

B5

Sub D1

20. (Amended) A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a diffusion barrier layer overlying the dielectric layer;

a gate electrode overlying the diffusion barrier layer;

a blocking layer overlying the gate electrode; and

two source/drain regions of second conductivity type formed on opposite sides of the channel region.

21. (Amended) A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

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Cont B5

a gate electrode overlying the dielectric layer; and

two source/drain regions of second conductivity type formed on opposite sides of the channel region, wherein the source/drain regions comprise silicon germanium.

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